PATENT APPLICATION #7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Frederick A. Ware, et al.

Title: METHOD AND APPARATUS FOR SIGNALING BETWEEN DEVICES OF A MEMORY SYSTEM

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Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT AND CLAIM UNDER 37 C.F.R. § 1.78

Dear Sir:

Please amend the above-identified application as follows:

In the Specification:

On page 2 of the specification, before line 1, please add the following paragraph:

This application is a continuation-in-part of patent application number 09/841,911, filed on 04/24/2001.

REMARKS

Applicant claims the benefit under 35 U.S.C. § 120 and 37 C.F.R. § 1.78 of the earlier filing date of patent application number 09/841,911, filed 04/24/2001, for all common subject matter.

Respectfully submitted,

02 Aug 02
Date

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same wire path as the bus. The subscripts (S,M) indicate the bus or clock signal at a particular module M or a particular slice S. The controller is defined to be slice zero.

The waveform for AClk clock signal 501 depicts the timing of the AClk clock signal at the memory controller component. A rising edge 502 of AClk clock signal 501 occurs at time 510 and is associated with the transmission of address information ACa 518. A rising edge 503 of AClk clock signal 501 occurs at time 511 and is associated with the transmission of address information ACb 519.

The waveform for AClk clock signal 520 depicts the timing of the AClk clock signal at a memory component located at slice one. The AClk signal 520 is delayed a delay of by t_{PD0} from signal 501. For example, the rising edge 523 of signal 520 is delayed by a delay of t_{PD0} from edge 502 of signal 501. The address information ACa 537 is associated with the rising edge 523 of signal 520. The address information ACb 538 is associated with the rising edge 525 of signal 520.

The waveform for AClk clock signal 539 depicts the timing of the AClk clock signal at the memory component located at slice N_S. The AClk signal 539 is delayed by a delay of t_{PD1} from signal 520. For example, the rising edge 541 of signal 539 is delayed by a delay of t_{PD1} from edge 523 of signal 520. The address information ACa 548 is associated with the rising edge 541 of signal 539. The address information ACb 549 is associated with the rising edge 542 of signal 539.

The clock signal AClk is shown with a cycle time that corresponds to the column cycle time. As previously mentioned, it could also have a shorter cycle time as long as the frequency and phase are constrained to allow the controller and memory components to generate the necessary timing points for sampling and driving the information on the bus. Likewise, the bus is shown with a single bit per wire transmitted per t_{CC} interval. As previously mentioned, more than one bit could be transferred in each t_{CC} interval since the controller and memory components are able to generate the necessary timing points for sampling and driving the information on the bus. Note that the actual drive point for

associated with write datum information Da 937. Rising edge 928 of signal 921 is associated with write datum information Dd 940.

The waveform RClk clock signal 929 depicts the RClk clock signal for the memory component at slice N_S at module one. Rising edge 932 of signal 929 is associated with read datum information Qb 938. Rising edge 933 of signal 929 is associated with read datum information Qc 939.

Note that in both Figures 8 and 9 there is a one t_{CC} cycle delay between the address/control information (ACa 917 of Figure 9, for example) and the read or write information that accompanies it (Da 937 of Figure 9 in this example) when viewed at each memory component. This may be different for other technologies; i.e. there may be a longer access delay. In general, the access delay for the write operation at the memory component should be equal or approximately equal to the access delay for the read operation in order to maximize the utilization of the data bus.

Figures 10 through 18 illustrate the details of an exemplary system which uses address and data timing relationships which are nearly identical to what has been described in Figures 5 through 9. In particular, all three clocks are in-phase on each memory component. This example system has several differences relative to this earlier description, however. First, two bits per wire are applied per t_{CC} interval on the AC bus (address/control bus, or simply address bus). Second, eight bits per wire are applied per t_{CC} interval on the DQ bus. Third, a clock signal accompanies the AC bus, but the read and write clocks for the DQ bus are synthesized from the clock for the AC bus.

Figure 10 is a block diagram illustrating further details for one memory rank (one or more slices of memory components) of a memory system such as that illustrated in Figure 1 in accordance with an embodiment of the invention. The internal blocks of the memory components making up this rank are connected to the external AC or DQ buses. The serialized data on these external buses is converted to or from parallel form on internal buses which connect to the memory core (the arrays of storage cells used to hold

1113 included in receive block 205. As a result, the serial information on the input 1016 is converted to parallel form on the output 1027.

Data receive block 205 comprises registers 1106, 1107, 1108, 1109, 1110, 1111, 1112, 1113, and 1114. Data input 1017 is coupled to registers 1106, 1107, 1108, 1109, 1110, 1111, 1112, and 1113, which are clocked by ClkM8 clock signal 1026 and coupled to register 1114 via couplings 1115, 1116, 1117, 1118, 1119, 1120, 1121, and 1122, respectively. Register 1114 is clocked by ClkM clock signal 1024 and provides write data to internal write data bus 1028. As a result, the serial information on the input 1017 is converted to parallel form on the output 1028.

Data transmit block 206 comprises registers 1123, 1124, 1125, 1126, 1127, 1128, 1129, 1130, and 1131. Read data from internal read data bus 1029 is provided to register 1131, which is clocked by ClkM clock 1024 and coupled to registers 1123, 1124, 1125, 1126, 1127, 1128, 1129, and 1130 via couplings 1132, 1133, 1134, 1135, 1136, 1137, 1138, and 1139. Registers 1123, 1124, 1125, 1126, 1127, 1128, 1129, and 1130 are clocked by ClkM8 clock 1026 and provide data output 1018. As a result, the parallel information on the input 1029 is converted to serial form on the output 1018.

Shown are the register elements needed to sample the address/control and write data, and to drive the read data. It is assumed in this example that two bits are transferred per address/control (AC[i]) wire in each t_{CC} interval, and that eight bits are transferred per read data (Q[i]) wire or write data (D[i]) wire in each t_{CC} interval. In addition to the primary clock ClkM (with a cycle time of t_{CC}), there are two other aligned clocks that are generated. There is ClkM2 (with a cycle time of $t_{CC}/2$) and ClkM8 (with a cycle time of $t_{CC}/8$). These higher frequency clocks shift information in to or out from the memory component. Once in each t_{CC} interval the serial data is transferred to or from a parallel register clocked by ClkM.

Note that ClkM2 and ClkM8 clocks are frequency locked and phase locked to the ClkM clock. The exact phase alignment of the two higher frequency clocks will depend

The frequency and phase adjustment is typically done with some type of phase-locked-loop (PLL) circuit, although other techniques are also possible. The feedback loop of the PLL circuit includes the skew of the clock drivers needed to distribute the various clocks to the receive and transmit blocks as well as the rest of the controller logic.

Figure 13 is a block diagram illustrating the logic used in the receive and transmit blocks of Figure 12 in accordance with an embodiment of the invention. Memory controller component 102 comprises address/control transmit blocks 201, data transmit blocks 202, and data receive blocks 203. For clarity, the elements for only one bit are illustrated. It is understood that such elements may be replicated for each bit of the buses.

Address/control transmit blocks 201 comprise register 1301 and registers 1302 and 1303. Internal address bus 1231 is coupled to register 1301, which is clocked by ClkC clock 1215 and provides outputs to registers 1302 and 1303 via couplings 1304 and 1305, respectively. Registers 1302 and 1303 are clocked by ClkC2 clock 1217 and provide output 1328 to the AC bus. As a result, the parallel information on the internal address bus 1231 is converted to serial form on the output 1228. Additional functional description of the address/control transmit blocks 201 is provided with respect to Figure 13 below.

Generally, the data transmit blocks 202 and data receive blocks 203 shown in Figure 13 serve the function of performing serial-to-parallel or parallel-to-serial conversion of data (the type of conversion depending upon the direction of the data flow). Such blocks are similar to those present within the memory devices, however in the case of the transmit and receive blocks included in the controller in this particular system, additional circuitry is required in order to obtain the appropriate clocking signals required to perform these serial-to-parallel and parallel-to-serial conversions. In the memory devices of this example, such clock adjustment circuitry is not required, as the clocks are understood to be phase aligned within the memory devices. However, within the controller such phase alignment cannot be guaranteed due to the assumption within the

the second memory component. The first wire connects to a first termination device. The second wire connects to a second termination device. The first wire maintains an approximately constant first impedance value along its full length on the memory module. The second wire maintains an approximately constant second impedance value along its full length on the memory module. The first termination component approximately matches the first impedance value. The second termination component approximately matches the second impedance value. Optionally, the first and/or second termination device is a component separate from the first memory component on the memory module. Optionally, the first and/or second termination device is a integrated into the first memory component on the memory module. Optionally, the first signal carries address information and the second signal carries data information. Such a memory module may be connected to a memory controller component and may be used in a memory system.

One embodiment of the invention provides a method for conducting memory operations in a memory system. The memory system includes a memory controller component and a rank of memory components. The memory components include slices. The slices include a first slice and a second slice. The memory controller component is coupled to conductors, including a common address bus connecting the memory controller component to the first slice and the second slice, a first data bus connecting the memory controller component to the first slice, and a second data bus connecting the memory controller component to the second slice. The first data bus is separate from the second data bus The method includes the step of providing a signal to one of the conductors. The signal may be an address signal, a write data signal, or a read data signal. The propagation delay of the one of the conductors is longer than an amount of time that an element of information represented by the signal is applied to that conductor. Optionally, the method may include the step of providing a first data signal to the first data bus and a second data signal to the second data bus. The first data signal relates specifically to the first slice and the second data signal relates specifically to the second slice. In one example, the first data signal carries data to or from the first slice, while the second data signal carries data to or from the second slice.

impedance which approximately matches an impedance of the termination resistors 3609 and 3613.

The termination structures may reside on the memory controller and memory component, or they may be placed separately on the module or main wiring boards near the memory controller and memory component. The termination resistors can be passive devices (for example, a discrete resistor component) or they may be an active device (for example, a transistor with circuitry to control its gate voltage such that it has a resistor-like transfer characteristic). This circuitry that controls the transfer characteristic may use a calibration process to keep the transfer characteristic near an optimal point. During such a calibration process, a value (such as a voltage) that represents the present transfer characteristic is first measured, and then another value (such as the contents of a configuration register) is adjusted to move the transfer characteristic closer to its optimal point. This calibration process is repeated periodically to ensure that variations in temperature, voltage, and process (e.g., variations arising during manufacture) have a minimal effect upon the effective transfer characteristic.

Control of a transfer characteristic refers to the ability to manage the output current versus the output voltage relationship of the output signal being transmitted by a component. If there is no control of this characteristic, then the current that is sunk by the driver at a particular output voltage can vary over a large range. Such variation can limit the maximum signaling bandwidth of the driver. If the current can be constrained, a higher signaling bandwidth is possible.

One way of controlling the transfer characteristic is to adjust the strength of the driver transistor. This can be done with parallel driver transistors with different weights (for example, binary weights may be used). This permits a set of discrete strengths of monotonically increasing value to be enabled selectively. A periodic calibration process controls this selection, first measuring a value that is indicative of the present transfer characteristic, and then adjusting the strength of the driver to move it closer to the optimal value. Other techniques for controlling the transfer characteristic are also

The pre-drivers for the address and control information in the memory controller 3901 also receive an enable signal EN at enable input 3916 which permits the drivers, exemplified by transistors 3908 and 3938, to turn off (e.g., transition to a high impedance state). The EN signal is used to drive address and control information at selected times, and to disable the driver at other selected times. The pre-drivers may also include circuitry that controls the slew rate of the drivers. The drivers may include circuitry that controls their transfer characteristic; for example, they may include circuitry to control their gate voltage such that it appears to be a current source with a relatively high source impedance. This circuitry that controls the slew rate or transfer characteristic may use a calibration process to keep the slew rate or transfer characteristic near an optimal point. During such a calibration process, a value (such as a voltage) that represents the present slew rate or transfer characteristic is first measured, and then another value (such as the contents of a configuration register) is adjusted to move the slew rate or transfer characteristic closer to its optimal point. This calibration process is repeated periodically to ensure that variations in temperature, voltage, and process (e.g., variations arising during manufacture) have a minimal effect upon the effective slew rate or transfer characteristic.

There is a termination structure at the memory component end of each of transmission lines 3920 and 3950 of the AC and ACN transmission line pair. These provide termination of signals representing address and control information traveling from memory controller 3901 to memory component 3902 along transmission lines 3920 and 3950. The termination structures at the far end (e.g., away from memory controller 3901) ensure that a wavefront is effectively absorbed after propagating down the transmission line once. As a result, there is negligible interference generated during a later wavefront. This allows the signaling rate of the wire to be maximized.

The address and control information is received at memory component 3902 by differential comparator 3914 of input receiver 3906. This circuit compares the voltages on transmission lines 3920 and 3950 of the AC and ACN wire pair. When the wire pair carries a valid signal, one wire will be at a higher voltage and the other will be at a lower

bus solution, but would permit the AC bus to be point-to-point like the DQ bus. Such an approach could potentially provide system benefits that would offset the increased pin cost (for example, it might allow easier routing of conductors on the main wiring board).

Bidirectional/Unidirectional Buses:

Typically, the information on the address and control bus flows only from memory controller to memory component, so the bus will be composed of unidirectional wires. In such a context, it is not necessary to provide a capacity for signals to flow from memory component to memory controller on this bus.

A data bus, such as those that have been described throughout this disclosure, may take a number of different forms. It may, for example, be implemented as a set of bidirectional wires that are used to send both read and write data (and any accompanying control and timing signals). In such an example, the read and write data propagate in opposite directions along individual wires of the data bus. The read data travels from the memory component to the memory controller, and the write data travels from the memory controller to the memory component.

Many bidirectional data buses require that read and write data not be simultaneously present because the transmit and receive circuitry on the memory component and controller component are not capable of handling overlapped bits (symbols).

However, there are some bidirectional buses which do permit the simultaneous presence of read and write data. This may be achieved by defining enough symbol encodings on a wire to support the four combinations of:

	Read Bit	Write Bit
(1)	0	0
(2)	0	1
(3)	1	0